

Part 1 of CPLD PLL Synthesizer

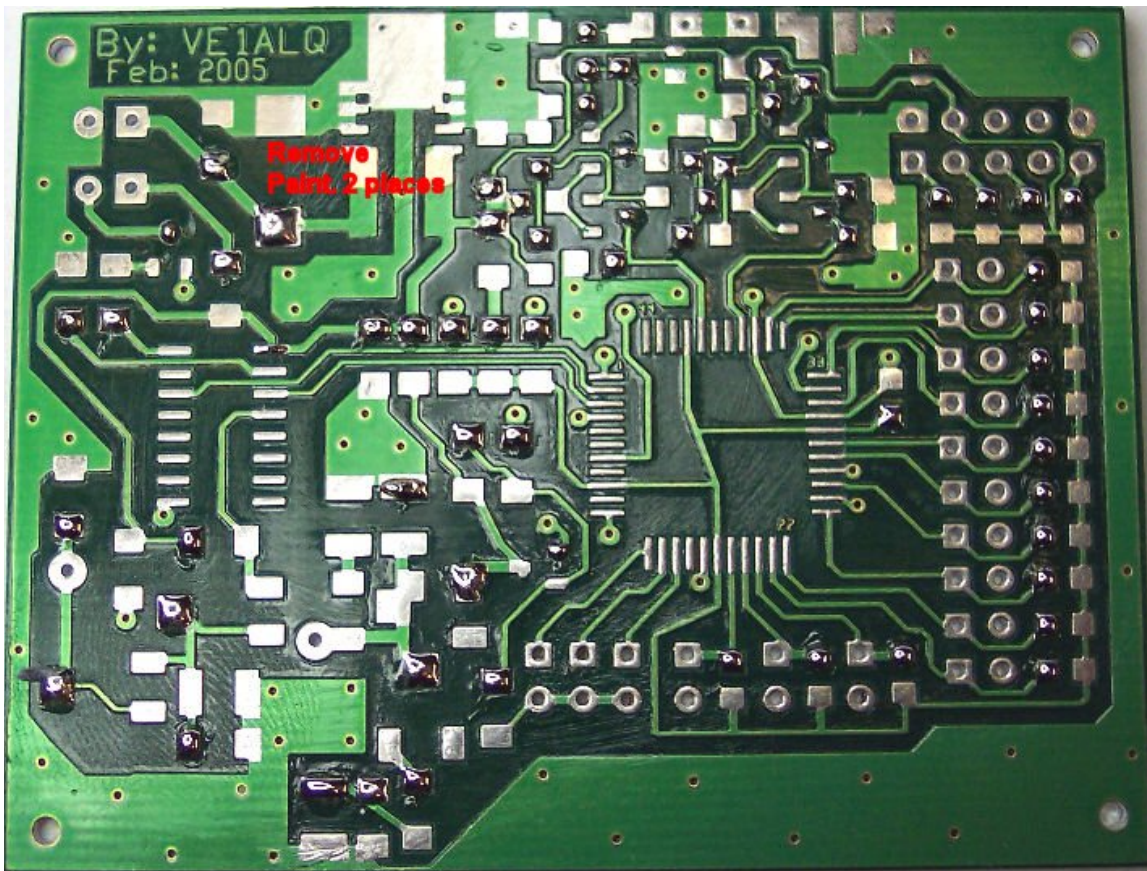
[Also See Part 2](#)

1/ [Placing Components.](#) 2/ [Voltage Verification 1.](#) 3/ [Resistance Verification.](#)
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Using a Q tip, or what ever you have, spread a Non Corrosive Solder Paste (Flux), I use Liquid Flux, on all solder pads.

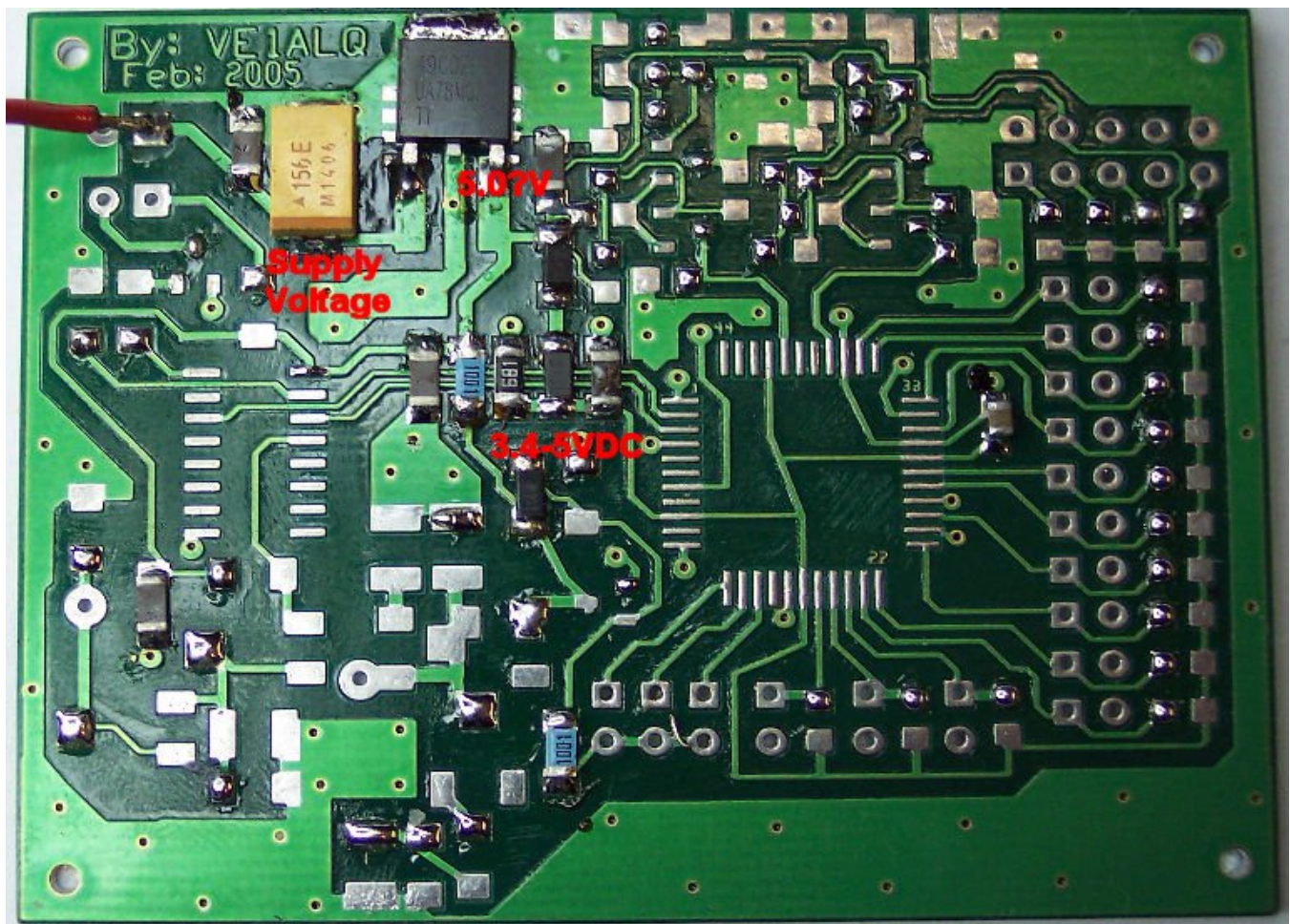
Suggested method of placing components is to simply place a small spot of Solder on one (1) end of each component placement pads as below, leaving the opposite pad for that component unsoldered. It is NOT recommend that additional Solder be applied to CPLD Pads at any time.

Before placement of the 78M05 Regulator, remove a small portion of Solder Mask as shown by *RED* label below and Solder Flux area.



Power Supply Components:

The first recommended step is to lay Power Components as shown below and verify Voltage as show. The actual level at these voltage points will vary slightly from Regulator, to Regulator, but will be close to that shown below. Note that the Second end of Component is NOW soldered in place, as components are placed.

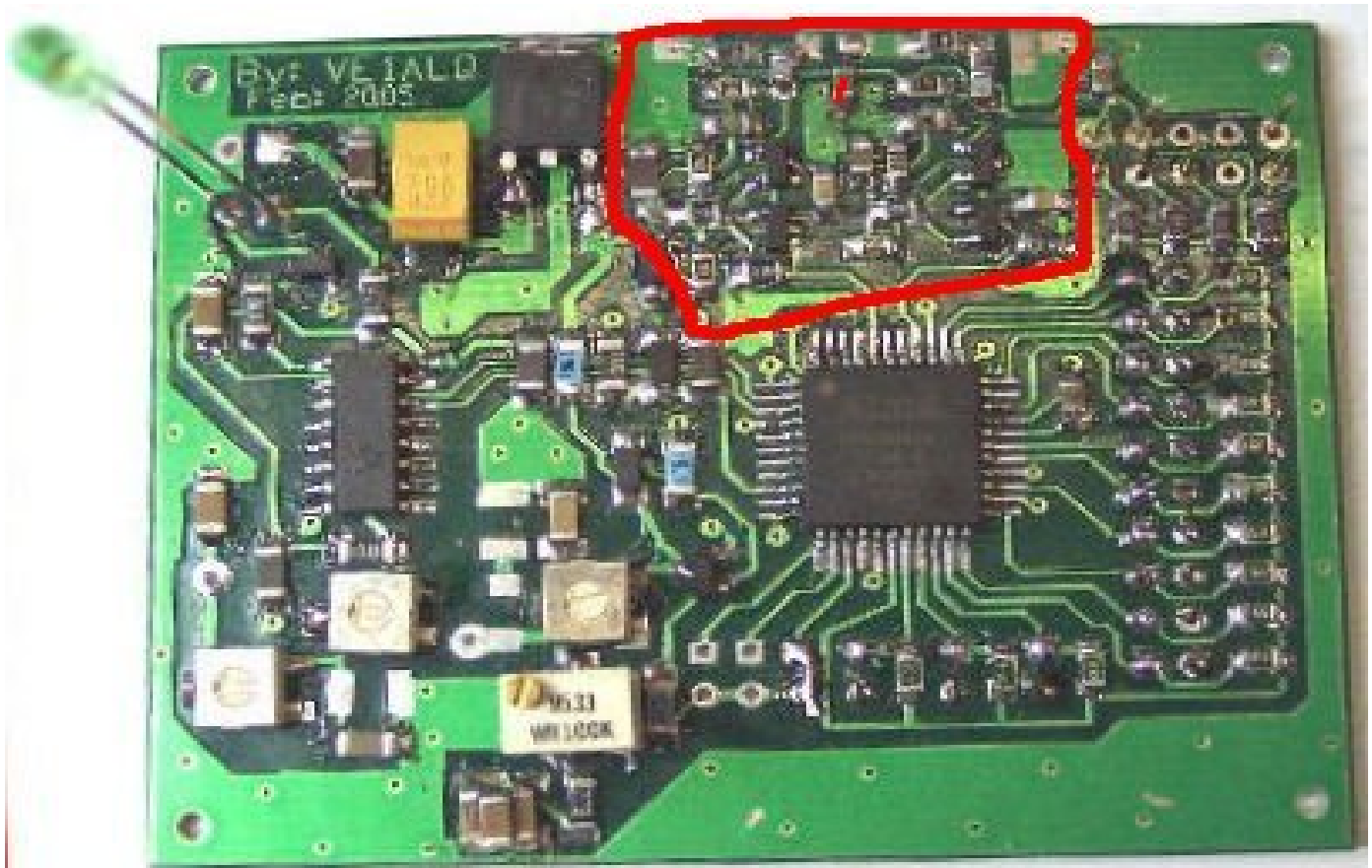


Voltages will be your Supply Voltage of 8 to 9 volts recommended. 5.0? At Regulator output, and 3.4 to 3.5 approx. as shown at the end of the second series diodes., or bottom of 680 Ohm resistor.

Passive Components;

It is now recommended that ALL Passive Components, resistors and capacitors, (NO PNP TRANSISTERS at this point), now be place at locations shown within the Red area below. The 0805 0.1uF capacitor shown with a RED line on it, I feel can and perhaps should NOT be installed, depending on if small Teflon Coaxial Line is used, or SMA Connector is used. I am now leaving it OFF the Boards. It is simply additional RF Filtering on the VCC1 (5.Volt) line and really NOT needed at that point.

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Again apply Supply Voltage and verify that there are approx. 5.0? Volts at the Emitter Junction End of each of the 2 X 150 Ohm resistors locations.

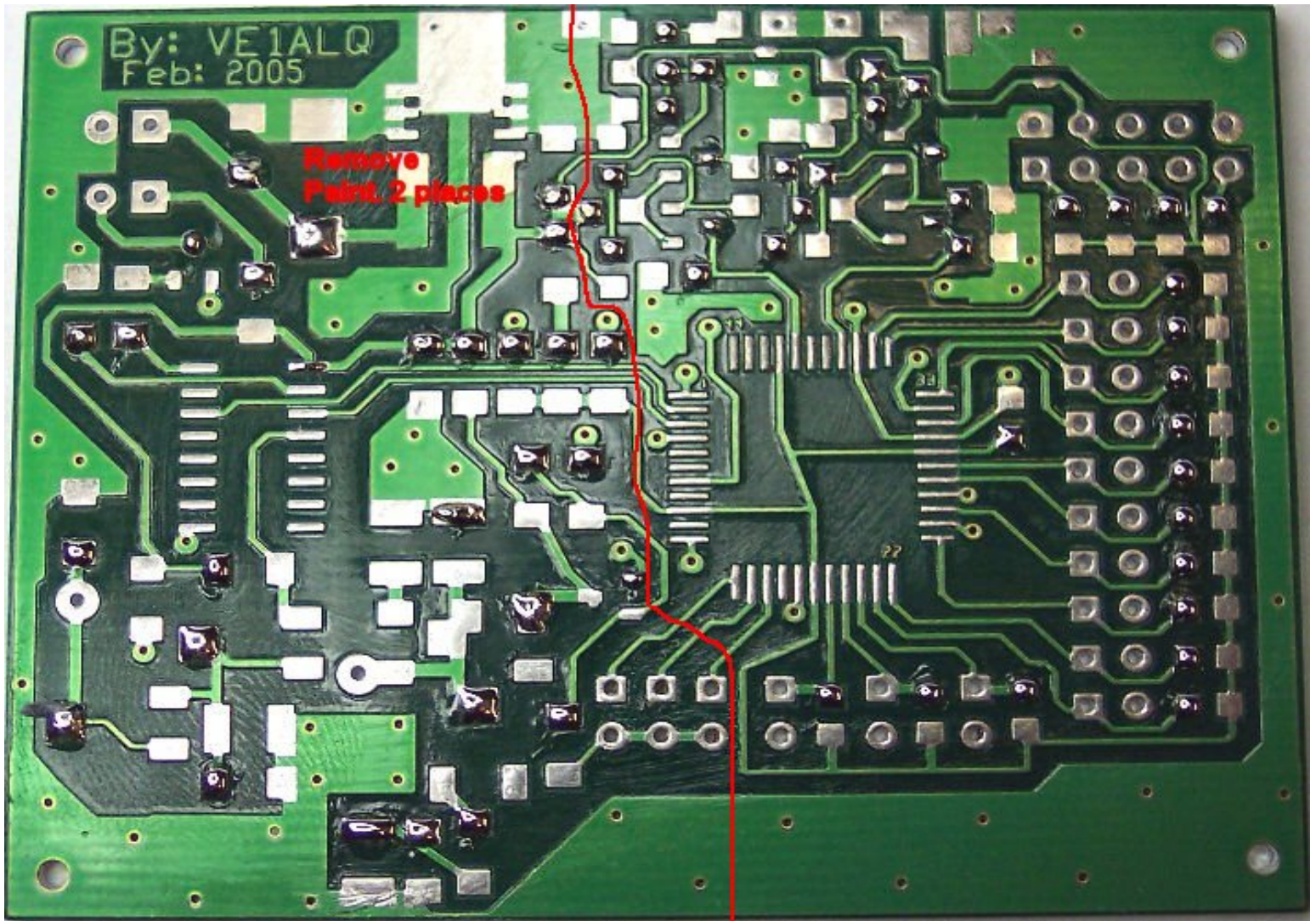
Verify approx. 2.5 Volts at each PNP Transistor Base location points, four (4) locations.

Continue to place Passive Components as per Silk Screen below, and verify your voltage as you feel it is appropriate.

NOTE: All Pull-up Resistors on the Binary Lines, Di1 to Di4 and n0 to n9 will be approx. 2.21K Resistors supplied with the Kit, and Pre-Assembled Boards and NOT the 1.2K as shown on the Silk Screen. These Pull-up Resistors and be 1.2 to 4.7K, higher values have NOT been verified.

The JTAG Pull-up Resistors will remain at 1.2K at the 10 Pin Connector locations.

No Passive Components, or Jumpers should be Installed at this point.



Following Installing of ALL Pull-up Resistors perform a Point to Point Resistance check, i.e. Inboard end of each installed resistor to VCC2 Line (junction of 680R and D3), and verify that the resistance value installed is in fact the value you read, +/- resistor tolerances.

There have been instances where the Silver Cap on a 0805 Size resistor has been found faulty and values read have been considerably higher (20 to 50K Ohms), than that of the resistor value installed creating real weird problems later.

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Continue now and install all six (6) Transistors, the 2 NPN and 4 X BFT92, but NOT the CPLD at this point. Make certain the BC847 and 2N2222 NPN is in the correct locations

Again Apply Supply Voltage of 8 to 13.8VDC and verify the following.

1/ Approx. 3.4V on the VCC2 Line at inboard end of each Pull-up Resistor.

2/ Approx. 3.6VDC at PNP Emitter Junction of the 150Ohm Resistor.

3/ Approx. 1.15 to 1.19 Volts on the 220Ohm Collector Input Resistor to CPLD.

4/ Approx. 2.6VDC at the each PNP Base decoupling Capacitors.

5/ Approx 2.5VDC at the PNP Base input coupling Capacitors.

These voltages are going to vary slightly depending on the actual Regulator Output Voltage, BUT MUST be close to that above. There has been BFT92 Transistors installed with relatively high internal leakage currents that displayed voltages considerably different than those shown above, making the PNP Transistor pair totally un-usable. Distorting the Waveform of either the Ref, or LO inputs, or even worse BOTH.

The LAST Active device to be installed should be the CPLD. **Since this Documents (Part 1), is not completed, and to get it on Site,** install all Active Devices including the CPLD.

Recommended procedure for installing the CPLD, since the Pads contain raised Solder Tinning from the Manufacture, is to simply place a very light coating of Flux over the Pads. Gently lay the CPLD, orientated as show, SQUARLY in the Pads Area, centering all 44 pins over their respective Pad. Using a 25W needle nose tipped Soldering Pencil; very lightly pull the existing Solder on the pads to the CPLD Pin, starting at the far point on the Pad from the CPLD toward the CPLD Pin. When the CPLD Pin is reached apply a very light downward pressure on the actual CPLD pin, imbedding in into the Solder securely.

1/ Before Applying Supply Voltage, **IMPORTANT:** Verify there are **NO SHORTS between ANY two (2) adjoining Pins on the CPLD.**

2/ Measure the Resistance to GROUND from VCC2 Line (680 Ohm Resistor) and confirm it is NOT less than the **680 Ohm resistor.**

3/ Measure the Resistance between the Regulator Output Pin and Ground, confirm NOT Less than **~450 Ohms.**

4/ Using an inline Current Meter Set for 200mA FULL SCALE in series with your Supply Voltage, apply your supply voltage and confirm current in the range of ~ 80mA NO devices being driven, no jumpers in place, but with CD74HC7046 installed. This current will increase as the Binary Jumpers are in place and pulling, in this case and additional ~1.5mA per jumper across a 2.21K Resistor. Also when Locked and Lock LED is Lit, etc, etc.

5/ Verify there is VCC2 voltage on the inward end of each Binary resistor and Ground.

Ok this May or May not be the last for this PDF, I am up in the air as to how to handle the VOM only approach Folks.

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Regards & Thanks, Darrell VE1ALQ at mail to: ve1alq@nbnet.nb.ca