

## BRIEF DESCRIPTION FOR CONNECTION THE VERSATILE PLL BOARD

1/ Voltage adjust should be set for 5VDC and may be changed during setup with VCXO Board.

2/ The First thing to be done is apply the Jumpers as required and in this case we will use a VCXO XTAL of 106.500000Mhz. See image below. The \*R\* Register is setup for a division of 40 and the \*N\* Register is Setup for a Division of  $426 - 1 = 425$

Enter XTAL Freq. in Hz	Ref. Osc. Mhz	XOR Comparator Freq. Khz	Enter Div. Ratio R Register
106500000	10	250.000000	40
<b>426.0000000000</b>			
<b>N Register</b>			
Now take N Register - 1 and convert this to Binary.		<b>425.00</b> <b>110101001</b>	<b>LSB</b>

**3cm** 189333333  
1000110111  
333.333333Khz

**6cm** 187200000  
1110100111  
Comparator 200.000Khz

**2304Mhz** 180.000000Mhz  
Comp. 200.0000Khz  
1110000011

**2320Mhz** 181.333333Mhz

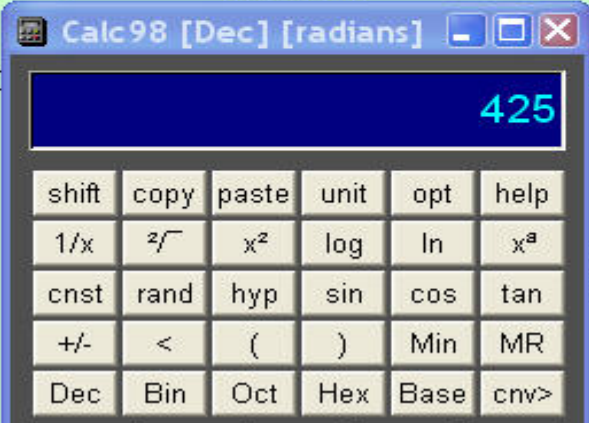
1 is C

ounded to 567  
9.333,333Mhz

**\*R\* REGISTER**

bove  
Ratio

**Versatile1  
"R" Register**  
100 = 000  
80 = 100  
75 = 010



Calc98 [Dec] [radians]

425

shift	copy	paste	unit	opt	help
1/x	z/√	x <sup>2</sup>	log	ln	x <sup>a</sup>
cnst	rand	hyp	sin	cos	tan
+/-	<	(	)	Min	MR
Dec	Bin	Oct	Hex	Base	cnv>

The 425 is then converted Binary as shown below (MSB 110101001 LSB) In this case Excel would have done it automatically because the number is less than 512, but I always use the Free Calc98. After entering the 425, press the BIN Button. PLEASE IGNORE ALL THE NUMBERS TO THE LEFT AND RIGHT OF THE Calc98.....Right now they mean nothing at all.

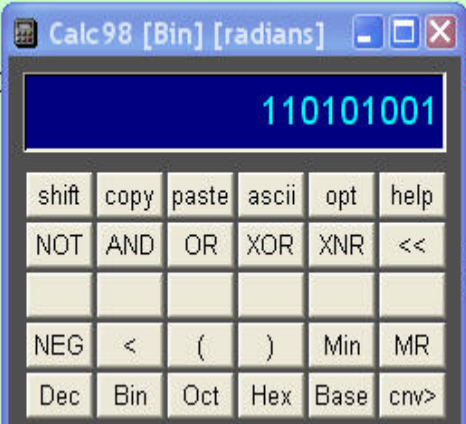
NEXT PAGE PLEASE

**Attempt to Derive at a NEARLY Even Number in the N Register by Selecting various R Register Division**

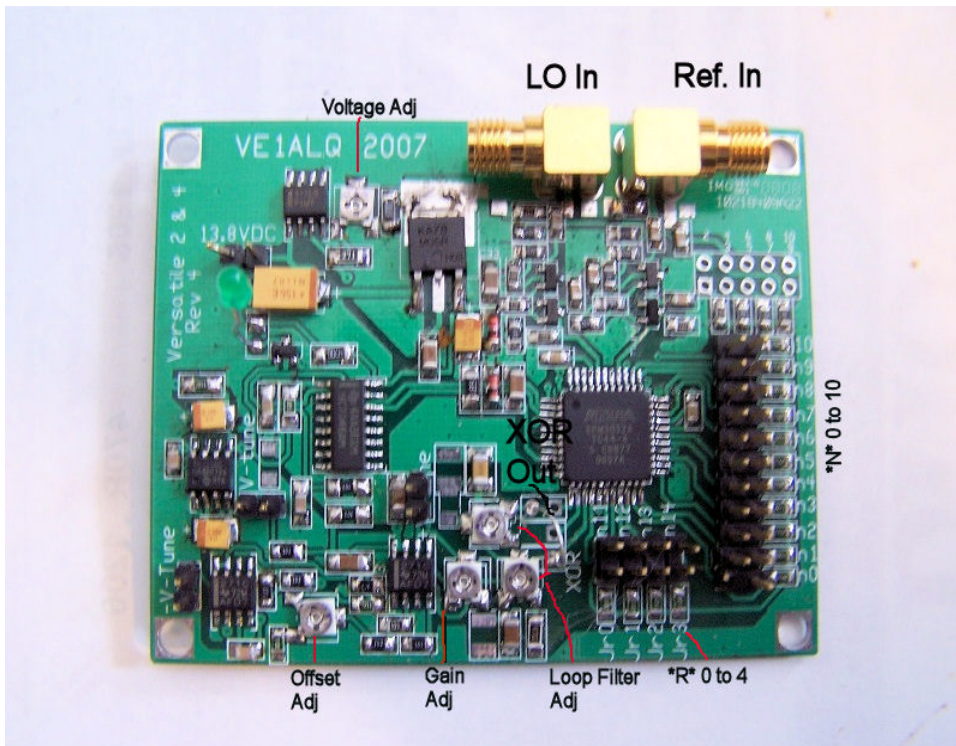
Enter XTAL Freq. in Hz	Ref. Osc. Mhz	XOR Comparator Freq. Khz	Enter Div. Ratio R Register	Versatile2
106500000	10	250.000000	40	100
426.000000000				95
<b>N Register</b>				90
				85
				80
				75
				70
				65
				60
Now take N Register - 1		425.00		55
and convert this to Binary.		110101001	LSB	50
				45
3cm 189333333				40
1000110111	1 is C			35
333.333333Khz				30
				25
6cm 187200000				
1110100111				
Comparator 200.000Khz				
2304Mhz 180.000000Mhz				
Comp. 200.0000Khz				
1110000011				
2320Mhz 181.333333Mhz				

Ratio	Versatile1 "R" Register	Versatile2 "R" Register
	100 = 000	100 = 0000
	80 = 100	95 = 0001
	75 = 010	90 = 0010



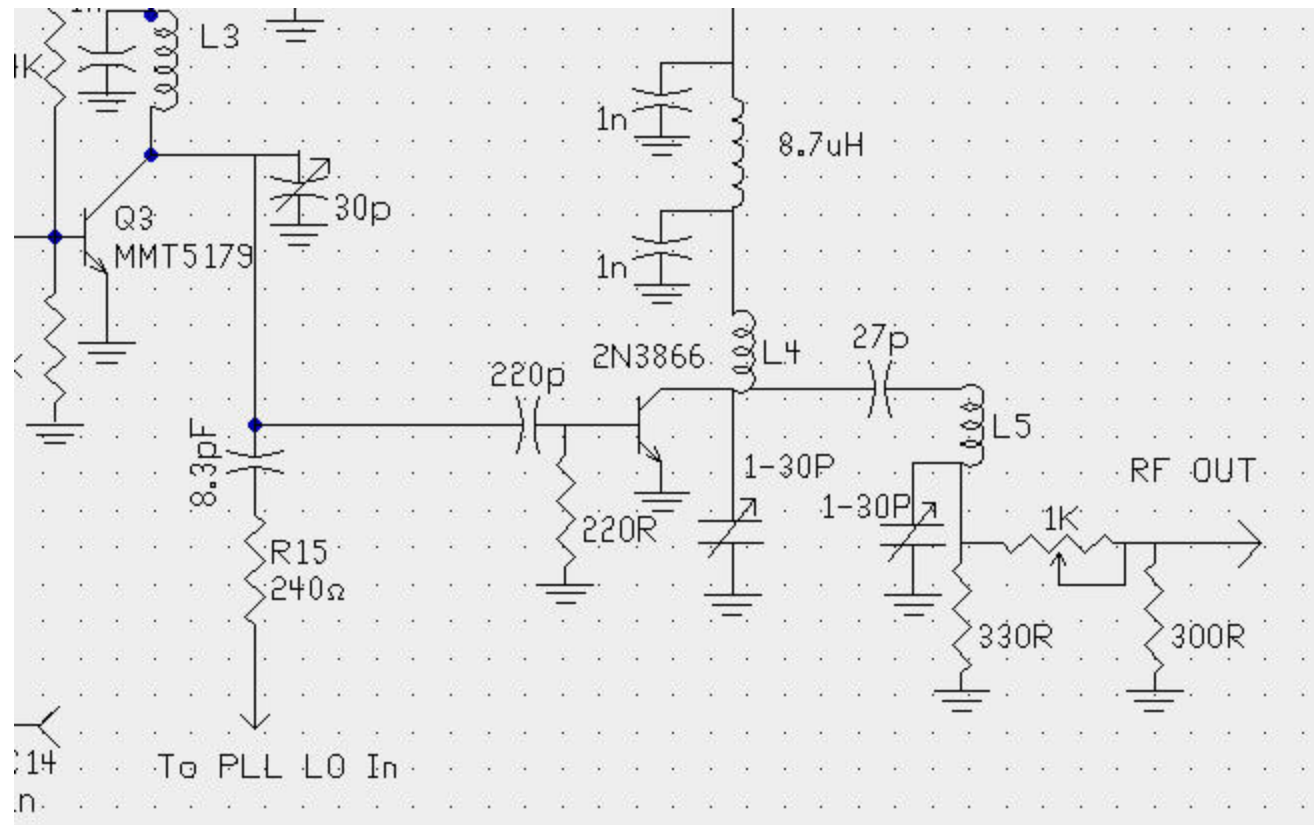
3/ now starting at the LSB (n0) to the MSB (n10) the Jumper are applied as shown above. 1= (open) and 0= (closed). The Binary above is showing 9Bits and there are actually 10Bits, therefore the 10<sup>th</sup> Bit is closed, or a jumper is placed on (n10).



3/ having placed all jumper CORRECTLY with the \*R\* register set for a division of 40 (0011) Jr0 to Jr3. And 13.8, or 9VDC applied to pins as shown at (13.8VDC) -12dbm of 10 MHz Ref. is connected to Ref. input and with a scope connected to the output XOR line you MUST see 1/2 of the XOR Freq. of 250Khz, or 125Khz. This is demonstrated at this location: <http://www.ve1alq.com/cpldpll/myvideoplayer.html>

4/ Once this is established, REMOVE the Ref. Freq. and connect your LO to the LO Port at approx. -12dbm and confirm that you see again 125Khz on the XOR line and it is showing no ringing and is very clean square wave with 50% duty cycle.

5/ to get this LO at a ~ -12dbm level I use a 8 to 10pF small Ceramic Capacitor in series with a 240 Ohm Resistor from a High Level point after the XTAL Osc. and before any Multiplication of the XTAL occurs. Resistor and capacitor values will vary from VCXO to VCXO depending on Design and designer  
 A Typical example shown below at R15.



This is my own VCXO above; the VCXO below is the typical DEMI MicroLO that is in use by many, where R9 is the pick off point.

This is an Image below displaying a complete Lock as indicated by the ~50% Duty Cycle, where both the Ref. Freq. and LO Freq. were divided to 100Khz. then combined at the XOR Line to 200Khz. Remember above when I indicated you will only see 1/2 of the TOTAL XOR Freq. with either the Ref. or LO connected, when both are connected the true XOR combined Freq.'s will be displayed. If your XTAL on the VCXO in 106.500000 MHz this will 250 KHz rather than 200Khz as shown





7/ referring to the DEMI MicroLO we can look at connecting the Varicap to an existing XTAL Osc. and at time this can become trial and error to some extent. To achieve accurate results, be sure to obtain a data sheet of the chosen Varicap and have a clear understanding of it's range and value with the applied minimum and maximum steering voltage before selecting the fixed value capacitor. Then, plug in the values, min and max to calculate the total capacitance swing.

An example would be a Varicap that varies from 12 pF @ 0.0 VDC to 2 pF @ 5.0 VDC in series with a 12 pF capacitor. This would produce a total capacitance swing of 6 pF maximum to a minimum of approximately 1.7 pf. The min/max values and range can be adjusted with different combinations of the two values. The important factors are that the minimum and maximums values do not exceed the oscillator's requirements for its optimum performance. If the range, high or low, can be adjusted to stop the oscillator from operating, there will not be any feedback to the reference lock circuit. This, in turn, will cause the control voltage to rail, high or low, not allowing the oscillator to start again. The circuit needs to be designed so it will remain oscillating at both minimum and maximum voltages that the reference lock circuit will source.

The next design desire will be the linearity of the swing. Although not as important, a smooth rate of frequency change per volt will make the circuit more reliable and have better frequency stability over temperature change. This is difficult to calculate but may be minimized by reducing the capacitance change per steering voltage swing. Now minimizing this swing to far may not allow the oscillator to start when cold, but if it is always used at a constant temperature or has some sort of "heater circuit", the oscillator will start and lock when it is within the "temperature window". The swing range may also be adjusted by designing a voltage divider on the control voltage line to minimize the voltage swing.

In the Circuit above I use a Gold plated variable capacitor to establish the approx. fixed capacitor, but using this approach there is the possibility of inducing Inductance as well which is NOT wanted. In most cases a small ATC Microwave Chip Cap in the range of 3 to 8pF should work quite well.

This Document can continue forever, dealing with XTAL Temperature turning point, motion capacitance, etc, etc, etc.

The intention was to leave you with the connections of the PLL to the VCXO and I believe that is covered quite well in this PART 1. If anyone has a question concerning the document, or needs more information please get in touch with me.

Mail to: [ve1alq@nbnet.nb.ca](mailto:ve1alq@nbnet.nb.ca)

Regards and Thanks for now, Darrell. VE1ALQ

**PART 2 will follow soon as possible and will deal with setting up the Loop Gain, Offset, and Voltage level**